A Reversible Ternary Adder for Quantum Computation

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Abstract. We present the design of a reversible ternary carry-ripple adder suitable for use with qutrits. Our design is based on the binary reversible adder of Vedral, Barenco and Ekert, and uses $3n + 1$ qutrits to add two n-trit numbers, with carry in and carry out. We assume a "rotor" gate as our basic gate.
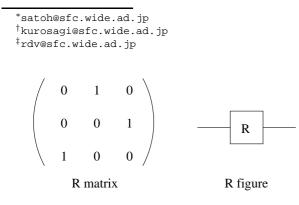
1 Introduction

Qutrits, ternary analogs to binary qubits, have been proposed for quantum communication, including quantum key distribution (QKD), and have been recognized as giving good spatial density for information storage [1, 2, 3]. Qutrits are three-state elementary quantum systems, defined by a basis set of three vectors. Much as qubits are defined using a basis set commonly written as $|0\rangle$ and $|1\rangle$, we define the basis set for ternary arithmetic to be $|0\rangle$, $|1\rangle$, and $|2\rangle$.

For any sort of complex computation on qutrits, we expect arithmetic subroutines to be an important component. Building blocks, including a full adder, have been defined [4], but larger, more complete circuits are also necessary. Therefore, we have designed a reversible ternary adder, based on the structure of the VBE carry-ripple adder circuit by Vedral, Barenco and Ekert [5]. Our circuit involves no uniquely quantum operations, and would be usable in a classical ternary logic context, which has a long if not exactly mainstream history [6, 7].

2 Concepts and Building Blocks

Our goal is to make a circuit that takes two n-qutrit numbers a and b and outputs a and $a + b$. In the following, we write the state of an n-qutrit register as $a = a_{n-1}3^{n-1} + a_{n-2}3^{n-2} + ... + a_1 3 + a_0$. Here, a_0 is the lowest-order qutrit, and a_{n-1} is the highest-order qutrit. Because our work is independent of the quantum nature of the trits, we dispense with the *ket* notation for the rest of this paper.

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We need a reversible ternary gate as our basic logic gate. We define a gate R we call the rotor. It takes $0 \rightarrow 1$, $1 \rightarrow 2$, and $2 \rightarrow 0$. Applying this gate three times to any trit will bring its state back to its original position. The unitary transform and graphical symbol for R are shown in Figure 1.

We also need a two-qutrit gate. The C-R gate, or control-R gate, rotates the second qutrit (the target qutrit) only if the first qutrit (the control qutrit) is 2, as shown in Figure 2. Similarly, the C-C-R gate rotates the third qutrit (the target qutrit) only if both of the control qutrits are 2.

2.1 SUM gate

The purpose of the ternary SUM gate, or block of gates, is the same as the purpose of the VBE binary SUM gate. This gate takes $(a_j, b_j, c_j) \rightarrow (a, c_j + a_j + b_j, c_j)$. a_j and c_j are undisturbed, while b_j becomes the sum of the three, modulo 3. c_j will be used as the carry from qutrit to qutrit in our overall circuit. The circuit for SUM is shown in Figure 3.
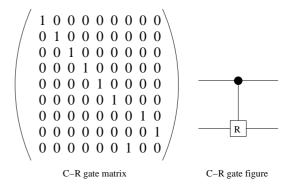

C–R gate matrix   C–R gate figure

Figure 2: The control-rotor gate.

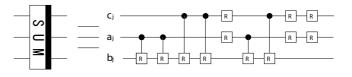Figure 3: The SUM gate.

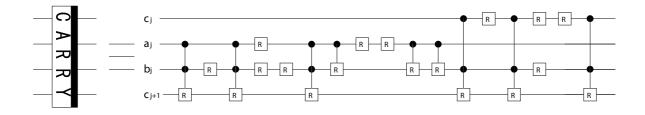R matrix   R figure
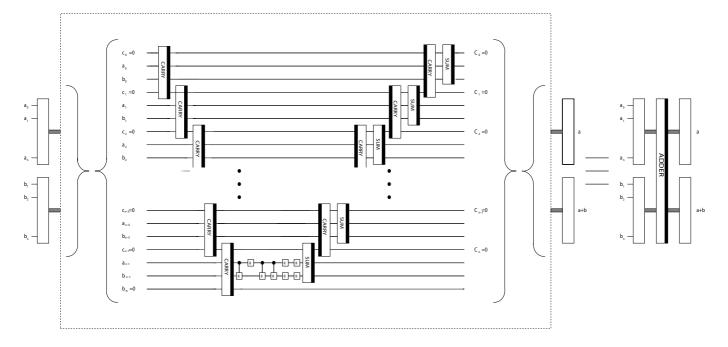
Figure 1: The rotor gate.

Figure 4: The CARRY gate.

Figure 5: The complete ternary carry-ripple adder.

2.2 CARRY gate

The purpose of the ternary CARRY gate is also the same as the purpose of the binary CARRY gate. CARRY outputs the carry c_{j+1} which is calculated when c_j, a_j and b_j are added.

3 The Reversible Ternary Adder

Our complete adder involves two n-qutrit registers, a and b, and n ancillae c, used to hold the intermediate carry values during the computation, and an additional qutrit b_{n+1} which holds the carry out, or new high digit of the b register. The adder leaves a undisturbed and takes $b \rightarrow a+b$. The c ancillae must be returned to their original zero state. As in the original VBE adder, the registers are interleaved, and the CARRY and SUM are arranged so that the carry qutrits are calculated in ascending order, a structure known as a carry-ripple adder.

The depth and total complexity of our circuit are both $O(n)$. Both the CARRY and SUM blocks for ternary logic are substantially longer than their binary equivalents. The exact performance will depend on the construction of three-qutrit gates.

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